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RISC-V cores and tools

SCR1 MICRO-CONTROLLER CORE

OVERVIEW

The SCR1 core is an open-source, RISC-V-compatible, 32-bit, entry-level microcontroller-class core, designed by Syntacore for general-purpose, deeply embedded applications and control systems.

This compact industry-grade IP core is based on the Harvard architecture with separate instruction and data buses and includes an in-order 4-stage pipeline, an IPIC unit, a TCM, industry-standard AXI4/AHB-Lite and JTAG/cJTAG interfaces. SCR1 is fully compliant with the RISC-V open instruction set architecture (ISA) defined by RISC-V International. The core can be configured for a very small area starting from 10k gates and is open-sourced under the permissive SHL license, which allows commercial use.

The core comes with pre-configured software tools and is ready for use out-of-the-box for commercial and educational purposes.

Figure 1 - Block diagram of the SCR1 processor

ADVANTAGES

- Open-source
- Compact size
- Low power-optimized
- Flexibility and customization
- High performance
- Suitable for educational purposes

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TECHNICAL SPECIFICATION

Feature	Description
ISA Support	RV32I/E[MC], Integer Multiplication and Division [M], Compressed Instructions [C] — optional
Execution Privilege Levels	Machine mode
Pipeline	In-order 2 – 4 stage pipeline (integer)
Hardware Multiplier/Divider	Speed-optimized/area-optimized
Optional Tightly-Coupled Memory (TCM)	I/D-shared, configurable: size - up to 64KB
Interrupt Support	IPIC - up to 16 interrupt lines, interrupt priority levels support
Embedded 64-bit RTC timer	Machine-mode timer interrupt support
Software Interrupts	Machine-mode software interrupt support
Low Power Management	Clock-gating support, power-gating support (coarse-grain power domain control, core-level UPF provided for low-power aware simulation and implementation), WFI (Wait For Interrupt) scheme to enter a sleep mode
Optional Debug Unit	JTAG/cJTAG-compliant interface, 2 hardware breakpoints, software breakpoints support
Advanced Performance Monitoring	2 performance counters
Bus Interfaces	Master AXI4 or AHB-Lite external memory interfaces

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BLOCK DIAGRAM

SCR1 has functional blocks included in the base configuration by default and optional blocks that can be added upon request during the development stage.

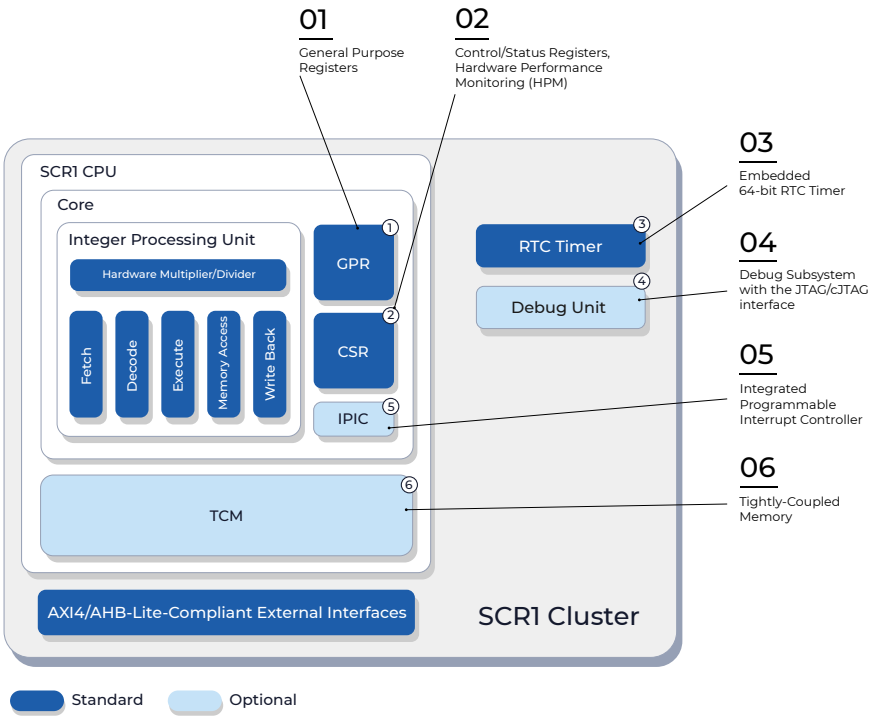

Figure 2 - SCR1 processor components

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CONFIGURATION OPTIONS

The SCR1 core platform offers wide customization possibilities with a default set of features that can be configured to meet your requirements.

Feature	Description
Instruction Set	RV32(I/IM/IMC/E/EM/EMC)
Hardware Multiplier/Divider	Speed-optimized/area-optimized according to requirements (iterative or pipelined configuration depending on frequency and performance requirements)
Optional Tightly-Coupled Memory (TCM)	4KB to 64KB
Interrupt Support	IPIC — up to 16 interrupt lines, interrupt priority levels support
Bus Interfaces	Master AXI with 32-bit data
	Master AHB-Lite with 32-bit data
Optional Debug Unit	Debug subsystem with the JTAG/cJTAG interface

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INSTRUCTION SET

Default

I/E: Base/Reduced Base Integer,

Zicsr: Control and Status Register Instructions,

Zifencei: Instruction-Fetch Fence

Optional

M: Integer Multiplication and Division,

C: Compressed Instructions

Figure 3 - SCR1 instruction set

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SOFTWARE

Syntacore develops and supports a wide range of tools optimized for SCR cores. This includes a ready-to-use package for software development (Syntacore Development Toolkit), a pre-built FPGA SDK, system software and detailed documentation. In addition, Syntacore provides an extensive support for third-party debugging hardware and software.

Syntacore Development Toolkit:

- Pre-built, tested and ready-to-use bundle
- Pre-configured and optimized for SCR cores
- Industry-quality toolchains support (GCC and LLVM)
- Support and regular release cycles
- Pre-configured OCD and GDB with Python scripts

Works out-of-the-box!

Software		Description
Syntacore Development Toolkit		
IDE		Visual Studio Code plugin
		Eclipse
Toolchain		GCC with binutils and Newlib libraries
		clang/LLVM compiler
Debuggers		GNU GDB
		OpenOCD
Simulator		QEMU
Software Examples		Sample applications and benchmarks
		Boards support package
Documentation		SDK User Guide, Tools Guide (IDE, CLI)
System Software		
OS		FreeRTOS/sel4/RTEMS/Mynewt/Zephyr
Bootloader and Firmware		First-stage bootloader/HAL
Third-Party Tools		
SEGGER	Probe	J-Link Ultra+
	IDE	Embedded Studio
Lauterbach	Probes	PowerDebug
		PowerTrace
	Debugger	Trace32
Ashling	Probe	Opella-XD
	IDE	RiscFree™
Digilent	Probe	JTAG-HS2
Olimex	Probes	ARM-USB-TINY-H
		ARM-USB-OCD-H

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DEVELOPMENT BOARDS

The SCR1 product package includes a ready-to-use FPGA development suite that features comprehensive documentation and pre-configured FPGA images. The package provides developers with an easy way to start working on their SCR1-based projects.

Supported FPGAs*

Manufacturer	Model
Digilent	ARTY A7-100T
AMD/XILINX	AMD Virtex UltraScale+ FPGA VCU118
Intel	Arria V GX
	Arria 10 GX

FPGA Resources Utilization**

FPGA	Configuration **SCR1 TCM 64KB**
Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit 1 182 240 LUTs / 2160 BRAM	0.52%/0.74%
Arty Nexys A7 (100T) 63 400 LUTs / 135 BRAM	9.88%/11.85%
Arria® 10 GX FPGA Development Kit 427 200 ALMs 55 562 240 RAM bits	0.89%/1.89%
Arria V GX FPGA Starter Kit 136 880 ALM 17 674 240 RAM bits	2.82%/5.94%

*Standard FPGA development boards supported by default. Customer FPGA images can be considered upon request.

**FPGA resources utilization by a RISC-V CPU cluster (base configuration).

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PRODUCT PACKAGE

The SCR1 product package includes:

Component	Contents
RISC-V Compatible Core	• System Verilog RTL source code
Syntacore Development Toolkit (downloaded separately)	• Toolchains • IDEs • Debuggers • Simulator • Software example projects
Comprehensive Documentation	• User Manual (quick start guide) • External Architecture Specification (EAS) • SDK User Guide • Tools Guide
FPGA-based SDK	• Sample FPGA projects • Pre-build FPGA images
Tests and Scripts for Simulation	• Verification test suite for pre-silicon (RTL simulation-based) • Verilator simulation support

Full RTL and supplementary collateral are available from the github repository.

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PERFORMANCE

			Configuration
			32-bit
Performance*, per MHz	**DMIPS**	-O2	1.53
		best**	2.76
	Coremark	best***	3.08
Area, kGates			11..40

Conditions: *Dhrystone 2.1, Coremark 1.0, LLVM-16-sc, run from TCM, **LLVM-16-sc OBest with LTO, ***LLVM-16-sc Obest with ground rules

CONTACT DETAILS

To learn more about the SCR1 core,
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NOTES

DS_SCR1 - v1