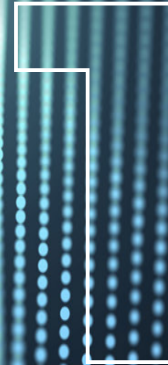




SCR1 MICRO- CONTROLLER CORE



OVERVIEW

The SCR1 core is an open-source, RISC-V-compatible, 32-bit, entry-level microcontroller-class core, designed by Syntacore for general-purpose, deeply embedded applications and control systems.

This compact industry-grade IP core is based on the Harvard architecture with separate instruction and data buses and includes an in-order 4-stage pipeline, an IPIC unit, a TCM, industry-standard AXI4/AHB-Lite and JTAG/cJTAG interfaces. SCR1 is fully compliant with the RISC-V open instruction set architecture (ISA) defined by RISC-V International. The core can be configured for a very small area starting from 10k gates and is open-sourced under the permissive SHL license, which allows commercial use.

The core comes with pre-configured software tools and is ready for use out-of-the-box for commercial and educational purposes.



Figure 1 - Block diagram of the SCR1 processor

ADVANTAGES

- [Open-source](#)
- Compact size
- Low power-optimized
- Flexibility and customization
- High performance
- Suitable for educational purposes

SCR1 MICROCONTROLLER CORE

TECHNICAL SPECIFICATION

Feature	Description
ISA Support	RV32I/E[MC], Integer Multiplication and Division [M], Compressed Instructions [C] — optional
Execution Privilege Levels	Machine mode
Pipeline	In-order 2 – 4 stage pipeline (integer)
Hardware Multiplier/Divider	Speed-optimized/area-optimized
Optional Tightly-Coupled Memory (TCM)	I/D-shared, configurable: size - up to 64KB
Interrupt Support	IPIC - up to 16 interrupt lines, interrupt priority levels support
Embedded 64-bit RTC timer	Machine-mode timer interrupt support
Software Interrupts	Machine-mode software interrupt support
Low Power Management	Clock-gating support, power-gating support (coarse-grain power domain control, core-level UPF provided for low-power aware simulation and implementation), WFI (Wait For Interrupt) scheme to enter a sleep mode
Optional Debug Unit	JTAG/cJTAG-compliant interface, 2 hardware breakpoints, software breakpoints support
Advanced Performance Monitoring	2 performance counters
Bus Interfaces	Master AXI4 or AHB-Lite external memory interfaces

SCR1 MICROCONTROLLER CORE

BLOCK DIAGRAM

SCR1 has functional blocks included in the base configuration by default and optional blocks that can be added upon request during the development stage.

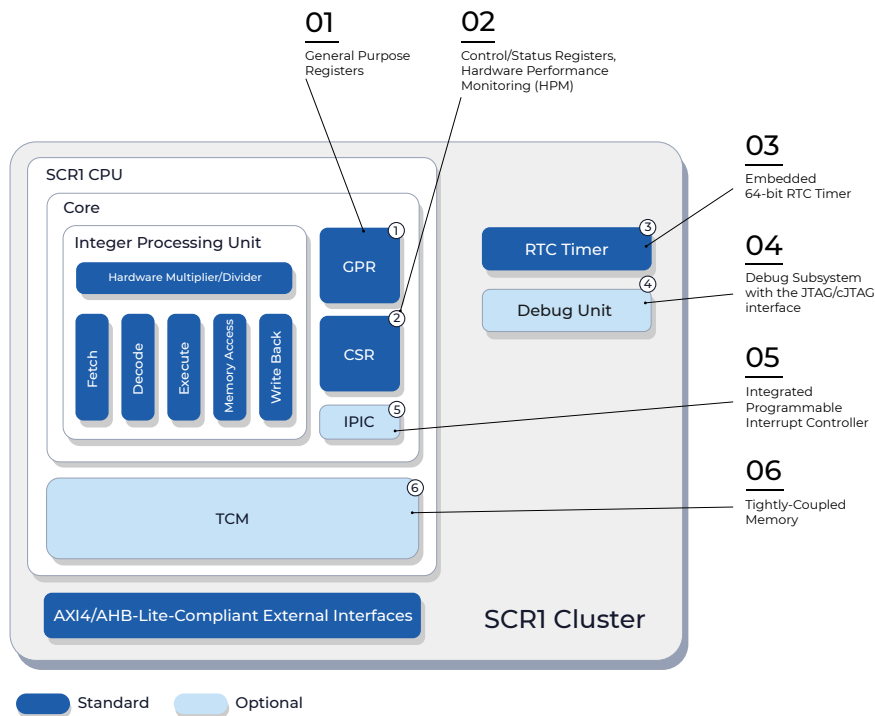


Figure 2 - SCR1 processor components

SCR1 MICROCONTROLLER CORE

CONFIGURATION OPTIONS

The SCR1 core platform offers wide customization possibilities with a default set of features that can be configured to meet your requirements.

Feature	Description
Instruction Set	RV32(I/IM/IMC/E/EM/EMC)
Hardware Multiplier/Divider	Speed-optimized/area-optimized according to requirements (iterative or pipelined configuration depending on frequency and performance requirements)
Optional Tightly-Coupled Memory (TCM)	4KB to 64KB
Interrupt Support	IPIC — up to 16 interrupt lines, interrupt priority levels support
Bus Interfaces	Master AXI with 32-bit data Master AHB-Lite with 32-bit data
Optional Debug Unit	Debug subsystem with the JTAG/cJTAG interface

SCR1 MICROCONTROLLER CORE



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INSTRUCTION SET

Default

I/E: Base/Reduced Base Integer,

Zicsr: Control and Status Register Instructions,

Zifencei: Instruction-Fetch Fence

Optional

M: Integer Multiplication and Division,

C: Compressed Instructions

RV32I/E and RV64I Base Integer/Reduced Base Integer and Custom ISA											
Base ISA	BEQ	XOR	LB	SB	SLL	ADD	LWU	SRAIW			
	BNE	XORI	LH	SH	SLLI	ADDI	LD	ADDW			
	BLT	OR	LBU	SW	SRL	SUB	SD	SUBW			
	BGE	ORI	LHU	SLT	SRLI	LUI	SLLI	SLW			
	BLTU	AND	LW	SLTI	SRA	AUIPC	SRLI	SRLW			
	BGEU	ANDI	FENCE	SLTU	SRAI	ECALL	SRAI	SRAW			
	JAL	JALR	FENCE.I	SLTIU	WFI	EBREAK	ADDI				
	CSRRW	CSRRC	CSRRSI	SFENCE.VMA	SRET	MRET	SLLIW				
	CSRRS	CSRRI	CSRRCI	CLFLUSH	CLNV	CLLOCK	SRLW				
											(in addition to RV32I)
Standard Extension ISA	RV32I/M Integer Multiplication and Division										
	MUL	MULHSU	DIV	REM			MULW	DIVW	REMUW		
	MULH	MULHU	DIVU	REMU			DIVW	REMW			(in addition to RV32M)
	RV32I/C Compressed Instructions										
	CMV	CLW	CSW	CBEQZ	CADD	CAND	CLD	CSD			
	CLI	CLWSP	CSWSP	CBEZ	CADDI	CANDI	CLDSP	CSDSP			
	CLUI	CFLW	CFSW	CJ	CADDI6SP	COR	CADDW	CSDW			
	C.SLLI	C.FLWSP	C.FSWSP	CJR	CADDI4SPN	C.XOR	CADDIW				
	CSRAI	C.FLD	C.FSD	CJAL	C.SUB	CEBREAK	C.SUBW				
	C.SRLI	C.FLDSP	C.FSDSP	C.JALR	C.NOP						(in addition to RV32C)
RV32I/64A Atomic Instructions											
LRW	AMOXOR.W	AMOMAX.W				LR.D	AMOXOR.D	AMOMAX.D			
SC.W	AMOAND.W	AMOMINU.W				SC.D	AMOAND.D	AMOMINU.D			
AMOSWAP.W	AMOOR.W	AMOMAXU.W				AMOSWAP.D	AMOOR.D	AMOMAXU.D			
AMOADD.W	AMOMIN.W					AMOADD.D	AMOMIN.D			(in addition to RV32A)	
RV32I/64F Single-Precision Floating-Point											
FLW	FNADD.S	FSQRT.S	FCVT.W.S	FLE.S	FSGNJX.S	FCVT.L.S					
FSW	FADD.S	FSGNJ.S	FCVT.WU.S	FCLASS.S		FCVT.LU.S					
FMADD.S	FSUB.S	FSGNJN.S	FMV.X.S	FCVT.S.W		FCVT.SL					
FMSUB.S	FMUL.S	FMIN.S	FEQ.S	FCVT.S.WU		FCVT.SLU					
FNMSUB.S	FDIV.S	FMAX.S	FLT.S	FMV.W.X						(in addition to RV32F)	
RV32I/64D Double-Precision Floating-Point											
FLD	FNADD.D	FSQRT.D	FMAX.D	FLE.D	FCVT.D.WU	FCVT.L.D	FMV.D.X				
FSD	FADD.D	FSGNJ.D	FCVT.S.D	FCLASS.D	FMV.2X.D	FCVT.LU.D					
FMADD.D	FSUB.D	FSGNJN.D	FCVT.D.S	FCVT.W.D	FMV.D.2X	FMV.X.D					
FMSUB.D	FMUL.D	FSGNJX.D	FEQ.D	FCVT.WU.D		FCVT.DL					
FNMSUB.D	FDIV.D	FMIN.D	FLT.D	FCVT.D.W		FCVT.D.LU				(in addition to RV32D)	
RV32						RV64					
RV32I/64V Vector Operations											
SEVL	VLD	AMOAND	VPLT	VPNOT	VMUL	VFMADD	VXOR	VMERGE			
VMULH	VLD.S	AMOOR	VPGE	VPSWAP	VDIV	VSGNJ	VOR	VSELECT			
VREM	VLDX	AMOMIN	VPAND	VMOV	VSQRT	VSGNDN	VAND	VST			
V.SLL	AMOSWAP	AMOMAX	VPANDN	VCVT	VFMADD	VSGNJX	VCLASS	VSTS			
VSRL	AMOADD	VPEQ	VPOR	VADD	VFMSUB	VMIN	VSETCFG	VSTX			
VSRA	AMOXOR	VPNE	VPXOR	VSUB	VFNMSUB	VMAX	VEXTRACT				
RV32I/64 Bit Manipulation											
CLMUL	SHADD.UW	MAX	ORCB	ROLW	SLLI.W	BCLRI	BSET	CTZW			
CLMULH	SH2ADD	MAXU	SEXT.B	ROR	ANDN	BEXT	BSETI	CPOP			
CLMULR	SH2ADD.UW	MIN	SEXT.H	RORI	ORN	BEXTI	CLZ	CPOPW			
ADD.UW	SH3ADD	MINU	ZEXT.H	BORIW	XNOR	BINV	CLZW				
SHIADD	SH5ADD.UW	REVB	ROL	RORW	BCLR	BINVI	CTZ				
RV64K Scalar Cryptography											
PACKH	SH2ADD.UW	AES64ES	AES64KS2	AES64IM	SHA256SUM0	SHA512SIGI					
PACK	XPERM8	AES64ESM	AES64DS	SHA256IG0	SHA256LM1	SHA512SUM0					
PACKW	XPERM4	AES64KSTI	AES64DSM	SHA256SIGI	SHA512SIG0	SHA512SUMI					

Figure 3 - SCR1 instruction set

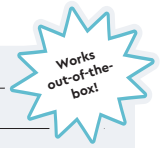
SCR1 MICROCONTROLLER CORE


SOFTWARE

Syntacore develops and supports a wide range of tools optimized for SCR cores. This includes a ready-to-use package for software development ([Syntacore Development Toolkit](#)), a pre-built FPGA SDK, system software and detailed documentation. In addition, Syntacore provides an extensive support for third-party debugging hardware and software.

Syntacore Development Toolkit:

- Pre-built, tested and ready-to-use bundle
- Pre-configured and optimized for SCR cores
- Industry-quality toolchains support (GCC and LLVM)
- Support and regular release cycles
- Pre-configured OCD and GDB with Python scripts



Software	Description	
Syntacore Development Toolkit 		
IDE	Visual Studio Code plugin Eclipse	
Toolchain	GCC with binutils and Newlib libraries clang/LLVM compiler	
Debuggers	GNU GDB OpenOCD	
Simulator	QEMU	
Software Examples	Sample applications and benchmarks Boards support package	
Documentation	SDK User Guide, Tools Guide (IDE, CLI)	
System Software		
OS	FreeRTOS/sel4/RTEMS/Mynewt/ Zephyr	
Bootloader and Firmware	First-stage bootloader/HAL	
Third-Party Tools		
SEGGER	Probe	J-Link Ultra+
	IDE	Embedded Studio
Lauterbach	Probes	PowerDebug PowerTrace
	Debugger	Trace32
Ashling	Probe	Opella-XD
	IDE	RiscFree™
Digilent	Probe	JTAG-HS2
Olimex	Probes	ARM-USB-TINY-H ARM-USB-OCD-H



SCRI MICROCONTROLLER CORE



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DEVELOPMENT BOARDS

The SCRI product package includes a ready-to-use FPGA development suite that features comprehensive documentation and pre-configured FPGA images. The package provides developers with an easy way to start working on their SCRI-based projects.

Supported FPGAs*

Manufacturer	Model
Digilent	ARTY A7-100T
AMD/XILINX	AMD Virtex UltraScale+ FPGA VCU118
Intel	Arria V GX Arria 10 GX

FPGA Resources Utilization**

FPGA	Configuration
	SCRI TCM 64KB
Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit 1182 240 LUTs / 2160 BRAM	0.52%/0.74%
Arty Nexys A7 (100T) 63 400 LUTs / 135 BRAM	9.88%/11.85%
Arria® 10 GX FPGA Development Kit 427 200 ALMs 55 562 240 RAM bits	0.89%/1.89%
Arria V GX FPGA Starter Kit 136 880 ALM 17 674 240 RAM bits	2.82%/5.94%

*Standard FPGA development boards supported by default. Customer FPGA images can be considered upon request.

**FPGA resources utilization by a RISC-V CPU cluster (base configuration).

SCR1 MICROCONTROLLER CORE

PRODUCT PACKAGE

The SCR1 product package includes:

Component	Contents
RISC-V Compatible Core	<ul style="list-style-type: none">• System Verilog RTL source code
Syntacore Development Toolkit (downloaded separately)	<ul style="list-style-type: none">• Toolchains• IDEs• Debuggers• Simulator• Software example projects
Comprehensive Documentation	<ul style="list-style-type: none">• User Manual (quick start guide)• External Architecture Specification (EAS)• SDK User Guide• Tools Guide
FPGA-based SDK	<ul style="list-style-type: none">• Sample FPGA projects• Pre-build FPGA images
Tests and Scripts for Simulation	<ul style="list-style-type: none">• Verification test suite for pre-silicon (RTL simulation-based)• Verilator simulation support

Full RTL and supplementary collateral are available from the [github repository](#).

SCR1 MICROCONTROLLER CORE



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PERFORMANCE

		Configuration	
		32-bit	
Performance*, per MHz	DMIPS	-O2	1.53
		best**	2.76
	Coremark	best***	3.08
Area, kGates			11.40

Conditions: *Dhrystone 2.1, Coremark 1.0, LLVM-16-sc, run from TCM, **LLVM-16-sc OBest with LTO, ***LLVM-16-sc Obest with ground rules

CONTACT DETAILS

To learn more about the SCR1 core,
contact Syntacore or visit the web:

<https://www.syntacore.com>

sales@syntacore.com



NOTES

DS_SCR1 - v1