SiFive

Welcome To The RISC-V Revolution!

Moscow, Russia
May 20, 2019

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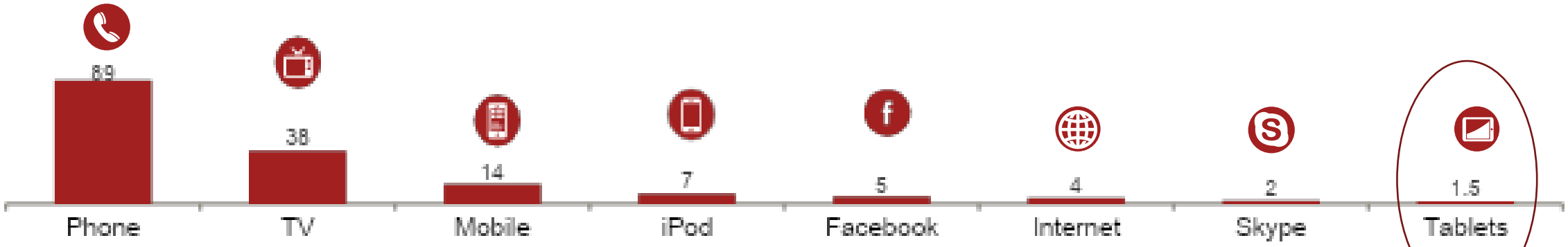
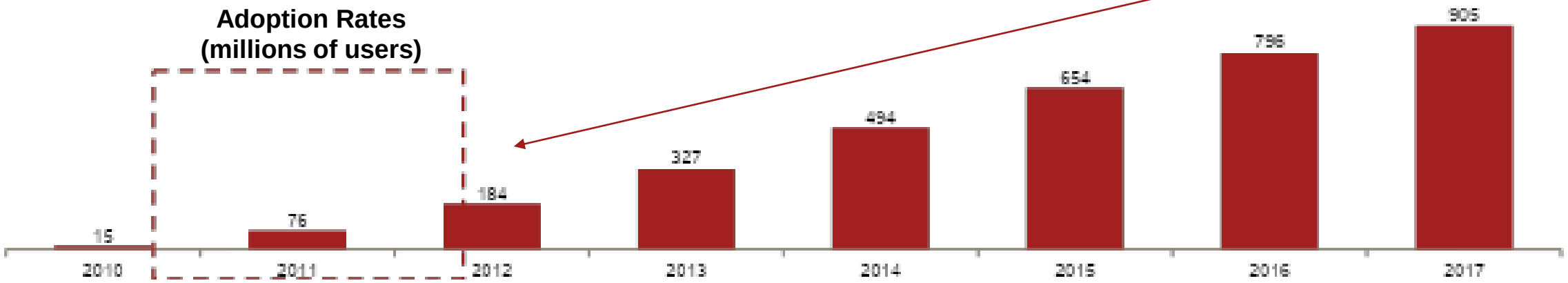
New Multi-Billion-Dollar Markets are Being Created in Quarters, Not Decades

Number of Years to reach 150 million total users

Fast Time to Market is a Competitive Advantage for Modern SOC Companies



Tablet/eReader Adoption Rates (millions of users)



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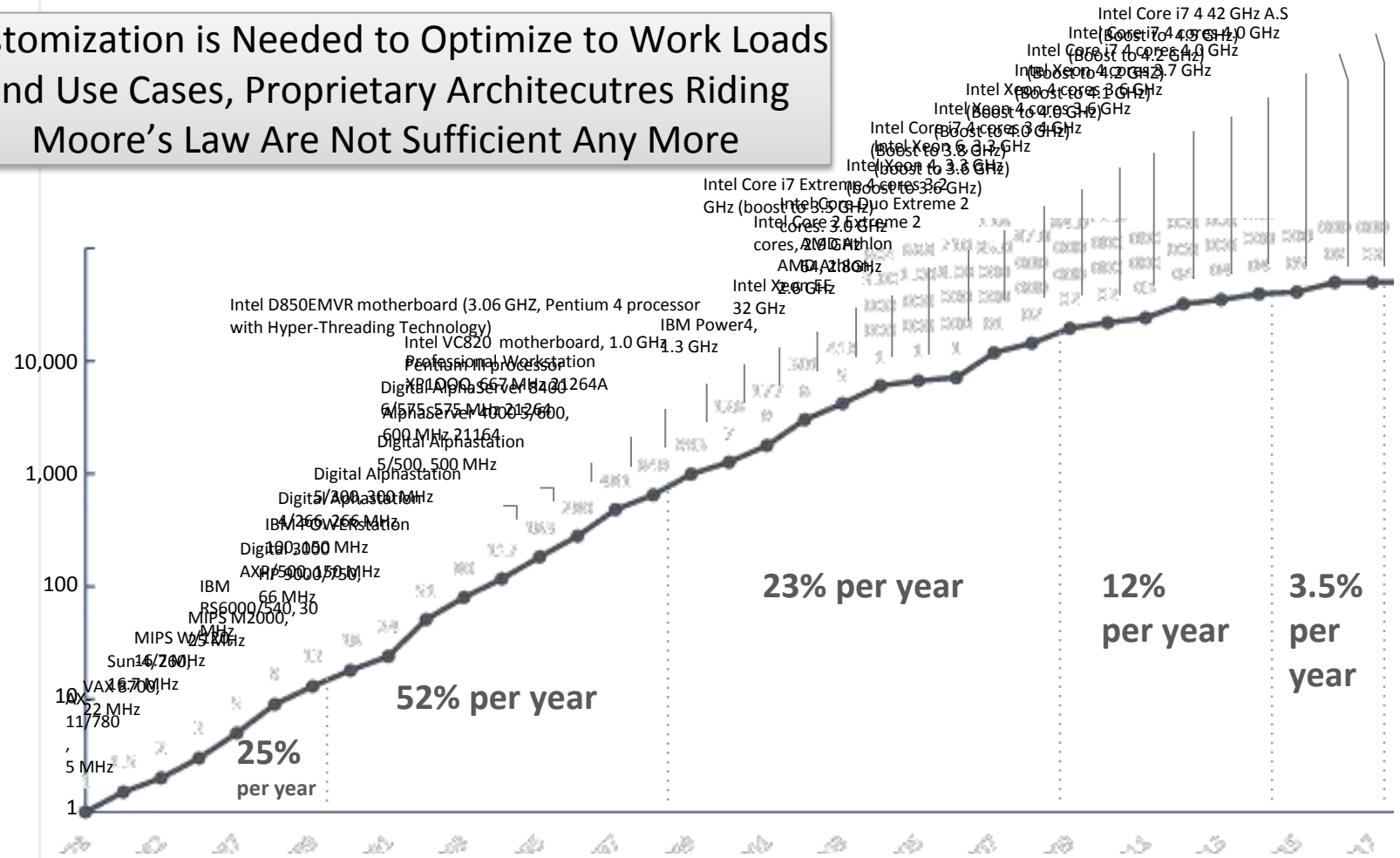
The Benefits of Moore's Law are Slowing; Moore's Law is Financially Failing

Moore's Law Has Stalled

General-purpose CPU performance (vs. VAX-11/780)

Customization is Needed to Optimize to Work Loads and Use Cases, Proprietary Architecutres Riding Moore's Law Are Not Sufficient Any More



Source: Hennessy, Patterson, Computer Architecture 6e

Time for a Paradigm Shift

Customization is the only way to get performance

One-Chip-Fits-All **no longer applies**

Innovation is desperately needed to meet the needs of new applications running on billions of devices

Agenda

09:00 – 10:00	Registration
10:00 – 10:10	Welcome and Introduction, by Jaspi Sandhu, VP of Sales, SiFive
10:10 – 10:50	RISC-V History and State of the Union, by Krste Asanovic, Chairman of RISC-V Foundation
10:50 – 11:10	Professional Development Tools for RISC-V, by Felipe Torrezan, FAE, IAR Systems
11:10 – 11:40	Keynote: Leading Semiconductor Design Revolution, by Krste Asanovic, Co-Founder and Chief Architect, SiFive
11:40 – 12:00	Break
12:00 – 12:20	SCRx Family of the RISC-V Compatible CPU IP, by Pavel Khabarov, Lead Engineer, Syntacore
12:20 – 12:40	Analytics, Tracing and Debugging Tools for the SoC Level for Projects Based on RISC-V, by Rupert Baines, CEO, UltraSoC
12:40 – 13:00	MicroTESK for RISC-V: Test Coverage Generation and Binary Code Analysis, by Alexander Kamkin, Lead Researcher, ISP RAS
13:00 – 14:00	Lunch and Demos
14:00 – 14:20	RISC-V Core IP for Target Vertical Markets, by Jahoor Vohra, Sr. FAE, SiFive
14:20 – 14:40	RISC-V Software Ecosystem Overview, by Syntacore
14:40 – 15:00	Freedom Revolution: Customizable RISC-V AI SoC Platform, by Krste Asanovic, Co-Founder and Chief Architect, SiFive
15:00 – 15:30	**Keynote:** Development of RISC-V in Russia, by Alexander Redkin, CEO, Syntacore
15:30 – 15:50	Break
15:50 – 16:15	**Tutorial:** SiFive Core Designer, by Jahoor Vohra, Sr. FAE, SiFive
16:15 – 16:40	**Tutorial:** Using SCR1 – Open RISC-V MCU Syntacore Kernel, Ekaterina Berezina, Senior HW Engineer, Syntacore
16:40 – 16:50	**Video:** Design Your Own CPU!!
16:50 – 17:00	Closing Remarks, by Alexander Redkin, Executive Director, Syntacore
17:00 – 18:00	Networking/Demos

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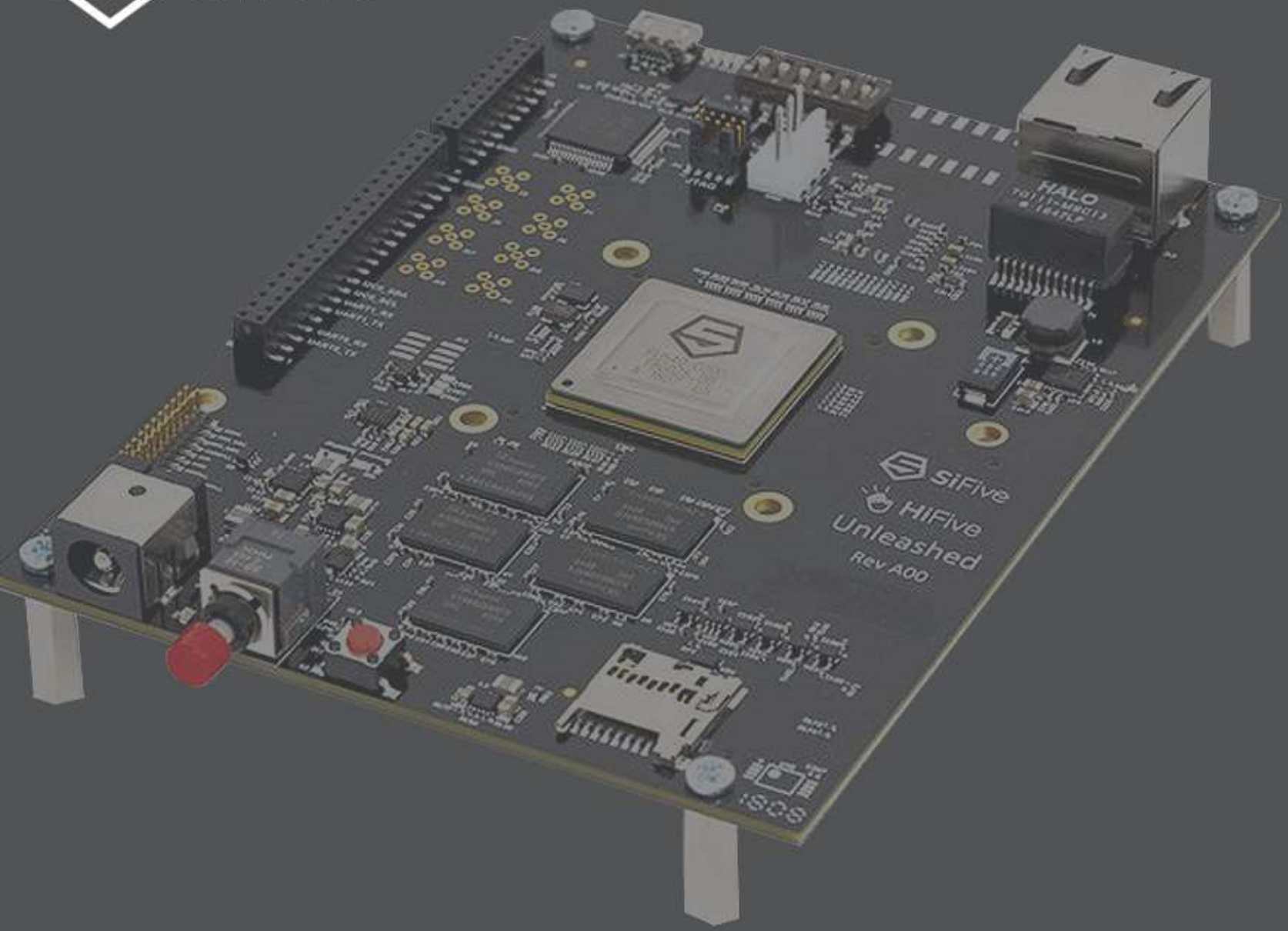

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The most advanced configurable core IP and silicon solutions from the inventors of RISC-V.

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