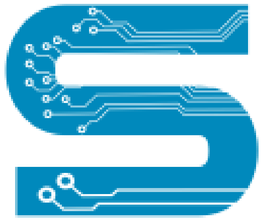

Syntacore™
Custom cores and tools

Программная инфраструктура RISC-V

Технический симпозиум RISC-V Москва
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  - IoT, RTOS
  - Kernels (Linux, BSD, others)
  - Операционные системы
  - Инструменты разработчика (toolchains, debuggers, etc)

ПО с открытым кодом

- GCC 8.3
- GNU Binutils 2.32
- Newlib 3.0.0
- GNU GDB 8.3
- Open On-Chip Debugger 0.10.0
- LLVM 5.0
- CompCert 3.1
- Glibc 2.29
- Free Pascal
- OpenJDK/HotSpot
- Go
- Ocaml 4.06
- V8
- Node.js
- Dart
- Rust

- Linux 4.x, 5.x
- FreeBSD
- NetBSD
- BusyBox
- BuildRoot
- Poky
- Gentoo
- Debian unstable
- Fedora
- seL4
- Zephyr
- RTEMS
- FreeRTOS
- Apache Mynewt
- coreboot
- Forth kernels
- etc...

Огромный интерес
и поддержка OpenSource
сообщества

Еженедельные обновления:
sw-dev@groups.riscv.org

Help wanted!

Примеры коммерческого ПО

ОС/симуляторы

- **ThreadX RTOS**
  https://rtos.com/solutions/threadx/
- **µC/OS-II**
  https://github.com/RISCV-on-Microsemi-FPGA/uCOS
- **Imperas** Multi Processor Debugger
  http://www.imperas.com/riscv#debug
- **OVPsim** multiprocessor platform emulator
  http://www.ovpworld.org/info_riscv

Инструменты разработчика

- **Segger Embedded Studio**

https://www.segger.com/products/development-tools/embedded-studio/

- **Lauterbach trace32**

https://www.lauterbach.com/frames.html?bdmriscv.html

- **IAR Embedded workbench**

https://www.iar.com/iar-embedded-workbench/tools-for-risc-v/

UltraSoC – Мощные комплексные средства отладки и профилирования уровня СнК:
https://www.ultrasoc.com/technology-2/risc-v/

RISC-V: Эмуляторы и симуляторы

Spike - RISC-V ISA simulator (riscv-isa-sim) considered to be the golden model of execution
https://github.com/riscv/riscv-isa-sim

QEMU - full system and user emulation (4.0.0, upstream)

http://qemu.org

RARS - RISC-V Assembler and Runtime Simulator

https://github.com/thethirdone/rars

TinyEMU (ex RISCVEMU) - RISC-V system emulator supporting the RV128IMAFDQC base ISA
https://bellard.org/riscvemu/

Renode - simulation framework
https://renode.io

ANGEL - JavaScript RISC-V ISA Simulator
https://riscv.org/software-tools/riscv-angel/

OVPsim (Imperas) multiprocessor platform emulator
http://www.ovpworld.org/riscv

Jor1k emulator written in JavaScript running Linux
https://github.com/s-macke/jor1k/

RISC-V: Мониторы и загрузчики

- **Coreboot** (upstream)
  https://review.coreboot.org/cgit/coreboot.git/
- **UEFI** (in progress)
- **Proxy Kernel/BBL** (runs on spike)
  https://github.com/riscv/riscv-pk
- **scbl** (SCR1 boot loader)
  https://github.com/syntacore/sc-bl

RISC-V: IoT, RTOS

- **Zephyr** 1.14 (upstream)
  https://www.zephyrproject.org
- **FreeRTOS** 10.2 (upstream)
  https://www.freertos.org
- **ThreadX RTOS** (upstream) - ExpressLogic/Microsoft
  https://rtos.com/solutions/threadx/
- **RTEMS** 4.11.3 (startus: works for RV32 and RV64, on Spike)
  https://www.rtems.org
- **µC/OS-II** (startus: ported)
  https://github.com/RISCV-on-Microsemi-FPGA/uCOS
- **Apache Mynewt** 1.6.0 (upstream)
  http://mynewt.apache.org

RISC-V: Kernels

- **Linux**:

Kernel 3.x, 4.x, 5.x (upstream)
https://www.kernel.org

- **BSD**:
  - FreeBSD (upstream 11.0)
    https://github.com/freebsd/freebsd
  - NetBSD (upstream)
    https://github.com/IIJ-NetBSD/netbsd-src

RISC-V: Kernels

- **Others**:
  - seL4 (64-bit port needs to go under seL4 team's review before getting officially released) https://github.com/heshamelmatary/seL4-riscv-mk
- **Forth** kernels:
  - muForth (status: upstream, initially targeting the SiFive FE310) https://github.com/nimblemachines/muforth
  - lbForth (status: upstream) https://github.com/larsbrinkhoff/lbForth

RISC-V: Операционные системы

Debian unstable (status: rv64 port)
https://wiki.debian.org/RISC-V

Fedora 28 (status: rv64 port, some changes upstreamed)
http://fedoraproject.org/wiki/Architectures/RISC-V

YoctoProject/OpenEmbedded (upstream)
https://github.com/riscv/meta-riscv

Gentoo (status: out of tree)
https://github.com/palmer-dabbelt/riscv-gentoo

FreeBSD 11.0 (status: base system, no ports yet)
https://github.com/freebsd/freebsd
https://wiki.freebsd.org/riscv

NetBSD

OpenSUSE (early preview)
https://en.opensuse.org/openSUSE:RISC-V

OpenMandriva (status: out of tree**)**

https://github.com/OpenMandrivaAssociation

RISC-V: Инструменты разработчика

Object toolchain

- **Binutils** 2.32 (upstream)
  https://github.com/riscv/riscv-binutils-gdb
- **LLVM** 8.0 (in progress)
  https://github.com/llvm-mirror/llvm

Debugging

- **GDB** 8.3 (upstream)
  https://github.com/riscv/riscv-binutils-gdb
- **OpenOCD** 0.10.0
  https://github.com/riscv/riscv-openocd
- **Imperas** Multi Processor Debugger
  http://www.imperas.com/riscv#debug

RISC-V: Инструменты разработчика

C compilers and libraries

- **GCC** 8.3 (upstream)
  https://github.com/riscv/riscv-gcc
- **LLVM/clang** (in progress)
- **CompCert** 3.5 (upstream)
  https://github.com/AbsInt/CompCert.git
- **Glibc** 2.29
  https://github.com/riscv/riscv-glibc
- **Newlib** 3.0.0 (upstream)
  https://github.com/riscv/riscv-newlib

RISC-V: Инструменты разработчика

Compilers and runtimes for other languages

- **Golang** (bootstrapped and passes tests, still missing cgo-related functionality, supports qemu and spike)
  https://github.com/riscv/riscv-go
- **Ocaml** 4.06 (out of tree)
  https://github.com/nojb/riscv-ocaml
- **Free Pascal** (out of tree)
  https://svn.freepascal.org/cgi-bin/viewvc.cgi/branches/laksen/riscv/trunk/
- **OpenJDK/HotSpot** (Java Virtual Machine, status: not yet public)
- **Jikes RVM** (Java Virtual Machine, status: not yet public)

Thank you!